

UK Semiconductor Infrastructure Initiative - Timeline

As part of the government's forthcoming National Semiconductor Strategy, the newly formed Department for Science, Innovation and Technology (DSIT) has commissioned a study to understand the technical and economic feasibility of developing specific capabilities to support commercial R&D, grow the UK semiconductor sector and contribute to supply chain resilience.

Across the project there are opportunities for stakeholders from across industry and academia to contribute to the project. This document provides an overview of the timeline for contributions.



IfM Engage Consortium

IfM Engage is leading this tender, forming the IfM Engage Consortium which is acting independently based on the Tender brief.

- All data collected (from surveys, discussions and interviews) are anonymous and protected.
- no comments will be attributed to individual companies without prior permission.

The IfM Engage Consortium

The central graphic displays the logos of the consortium members. At the top left is the UK Government crest with the text 'Funded by UK Government'. To its right is the 'IfM Engage' logo, with the subtext 'Part of the Institute for Manufacturing'. Further right is the 'Cambridge Econometrics' logo with the tagline 'clarity from complexity'. Below these are the logos for 'Si SILICON CATALYST', 'TechWorks', 'nmi', 'CATAPULT Compound Semiconductor Applications', and 'PHOTONICS LEADERSHIP GROUP'. The bottom row includes 'SEMIWISE', 'FutureHorizons The Global Semiconductor Industry Analysts' (with a satellite icon), 'Imperial College London', and 'UNIVERSITY OF LEEDS'.

Work Packages

The tender brief specifies the project focusses on five work packages:

- WP1 - Silicon manufacturing capability to support prototyping
- WP2 - Compound open-access foundry capability
- WP3 - Advanced packaging capability
- WP4 - Design IP/tooling capability
- WP5 - Strategic coordination capability that would provide an institutional framework around the infrastructure components



DSIT Tender Brief

- WP1 Silicon Prototyping
- WP2 Compound foundry
- WP3 Advanced Packaging
- WP4 Design Tools and IP
- WP5 Institutional Framework

UK Semiconductor Infrastructure Initiative – Summary Timeline

Review of International best practice to inform the appropriate institutional framework to deliver these capabilities

Econometric analysis to provide evidence to inform the economic & financial case
Selection and costing of intervention scenarios

April – November 2023



Design and planning

1st survey launched to collect User Needs

2nd survey launched to map Existing Infrastructure

Workshops to validate survey findings

Visits to all UK Semiconductor clusters

Consultation with major UK end users

March 2023

May 2023

June 2023

July 2023

September 2023

October 2023

- Methodology refinement
- Survey design
- Contacts identification
- Logistics

- Invited participation from >180 UK organisations
- Open invitation to all interested organisations via online platforms

- Invited participation from >30 UK organisations
- Open invitation to all interested organisations via online platforms

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- Analysis of needs and capabilities
- Proposed methods of intervention

- Face-to-face visits to all UK Semiconductor clusters
- Intervention scenarios
- Discussion preferences

- Identify potential interest of major UK end users on supporting the infrastructure initiative
- Prioritisation of intervention scenarios
- Report to DSIT

Government analysis
Decisions
Implementations



For more information

To participate in the project, visit:

- engage.ifm.eng.cam.ac.uk/uk-semiconductor-infrastructure-initiative-2023

- Or scan the QR code



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